Name and Std No.: Riley Lawson 116555487 Lab Section: 6

Date: 10/29/2020

**Submission Instructions:**

**Prelab:**

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

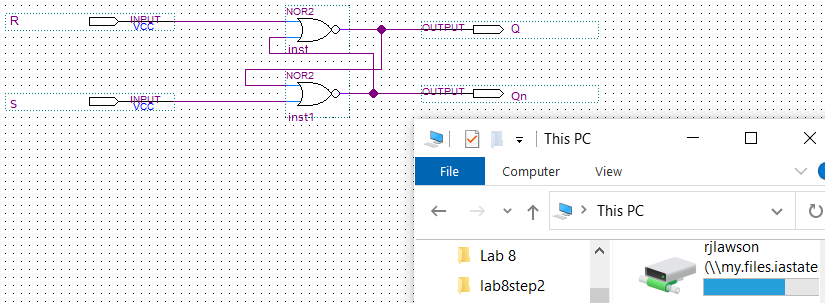
**Lab:**

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

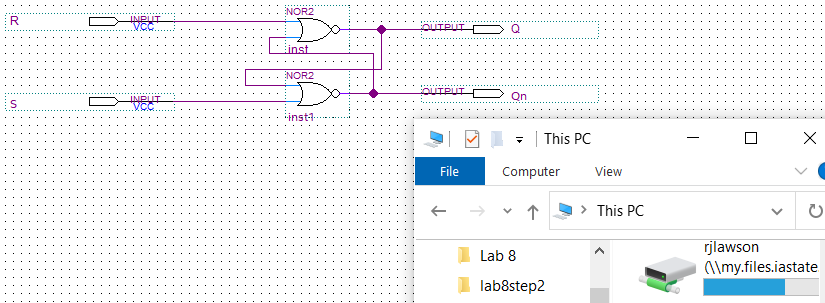
**PRELAB:**

### *Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.*

**Q1.** Draw the circuit diagram for the SR Latch using NOR Gates for **Section 2.0** in the space below.



**Q2.** Draw the circuit diagram for the SR Latch using NAND Gates for **Section 2.0** in the space below.

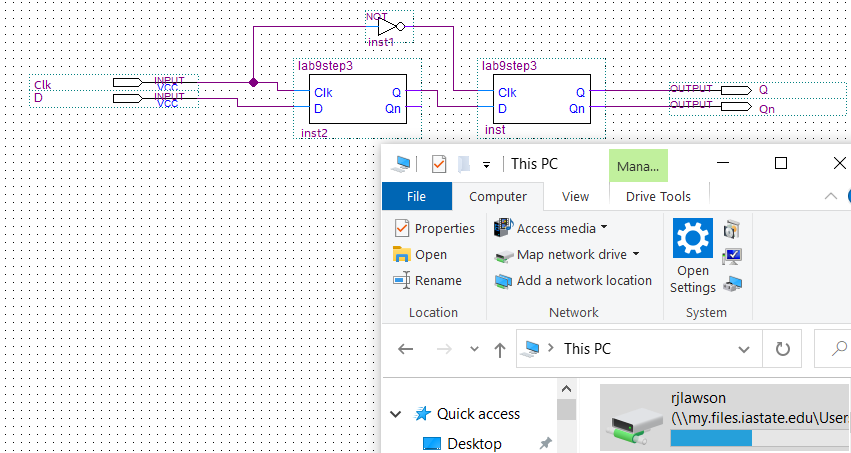


**Q3.** Draw the circuit diagram for the D Latch using NAND Gates and a NOT gate for **Section 3.0** in the space below.

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**Q4.** Draw the circuit diagram for the Master-Slave D Flip-Flop for **Section 4.0** using the D latches you built in the previous step in the space below. The flip-flop should be triggered by the negative edge of the clock.

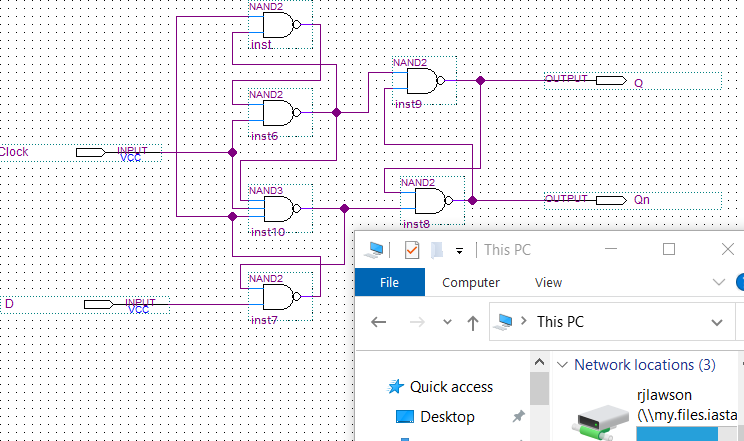
**FIXED!**

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**Q5.** Draw the circuit diagram for the Positive-Edge-Triggered D Flip-Flop using NAND gates for **Section 4.0** in the space below.

**FIXED!**



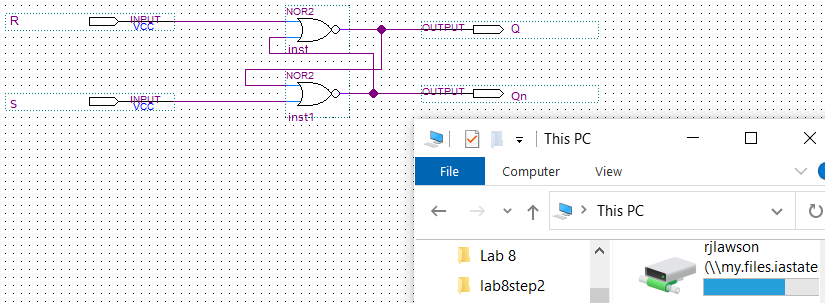
**LAB:**

**2.0** Complete the characteristic table for both versions of the SR latch. Do both versions function properly as a latch?

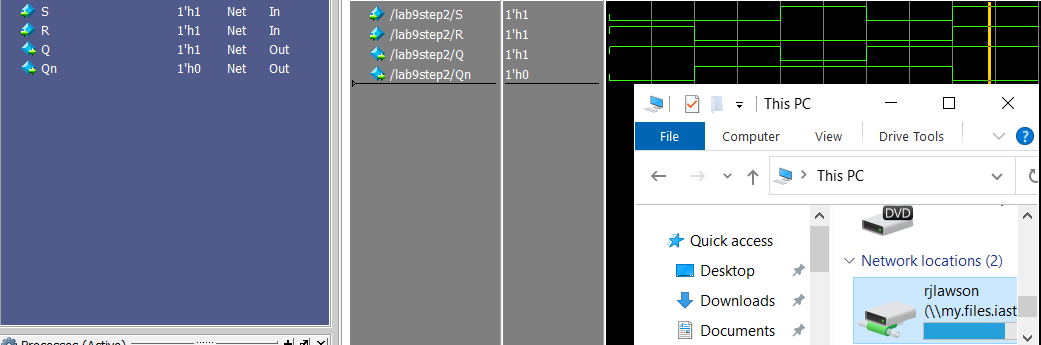
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SR NOR Latch** | |  | **SR NAND Latch** | |
| **S R** | **Action** |  | **S R** | **Action** |
| 0 0 | *Keep State* |  | 0 0 | *Keep State* |
| 0 1 | *Q = 0* |  | 0 1 | *Q = 1* |
| 1 0 | *Q = 1* |  | 1 0 | *Q = 0* |
| 1 1 | *Restricted Combination* |  | 1 1 | *Restricted Combination* |

**NOR Screenshots:**

<<<Insert a screenshot of your SR NOR latch here>>>

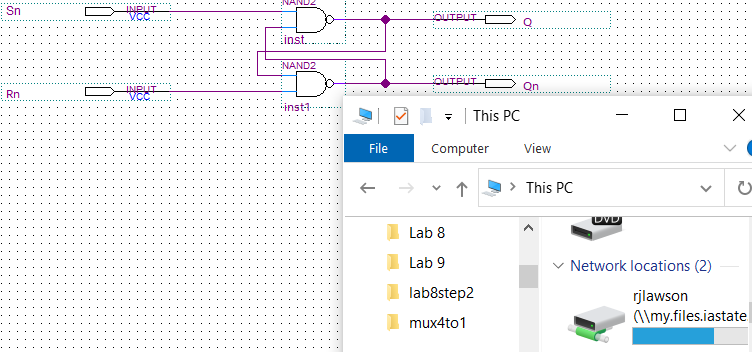


<<< Insert a screenshot of your waveform for your SR NOR latch here>>>

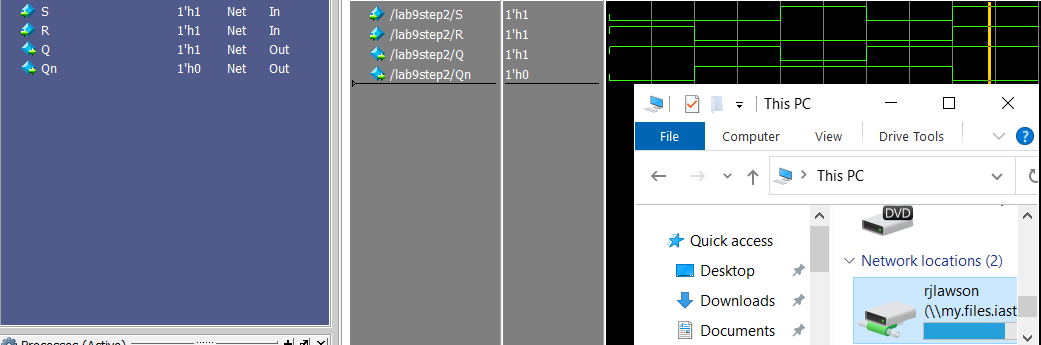
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**NAND screenshots:**

<<<Insert a screenshot of your SR NAND latch here>>>



<<< Insert a screenshot of your waveform for your SR NAND latch here>>>

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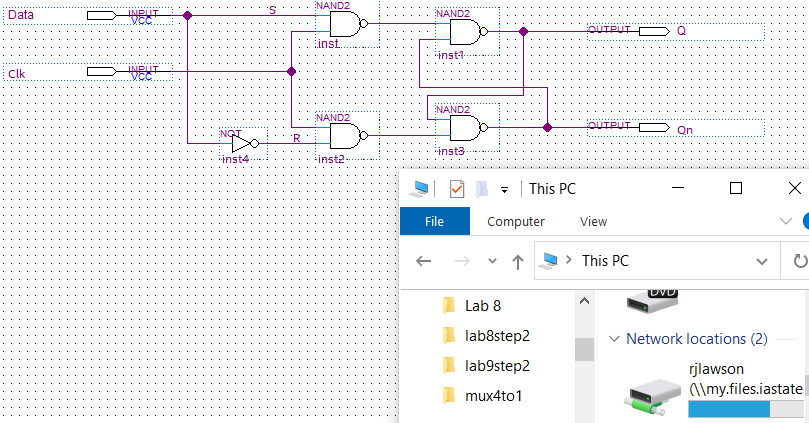
**3.0** Complete the timing diagram below for your Gated D Latch. What is the difference between this gated latch and the previous basic latches?

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** | - | \_ | - | - | - | - | - | \_ | \_ | \_ | \_ | \_ | - | \_ | \_ | \_ | \_ | \_ | - | - | - |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

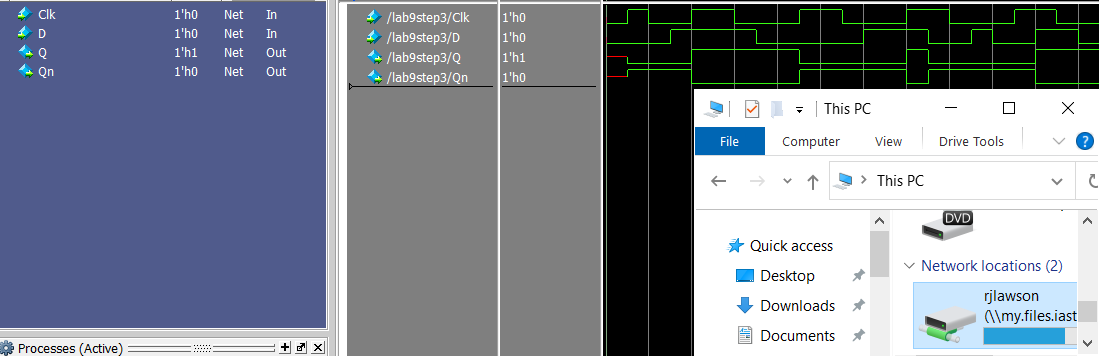
A gated D latch only has 1 input variable (besides the clock) and has a clock signal that is consistent, whereas the basic latches has two inputs that determine the output

**D Latch Screenshots:**

<<<Insert a screenshot of your D latch here>>>



<<< Insert a screenshot of your waveform for your D latch here>>>

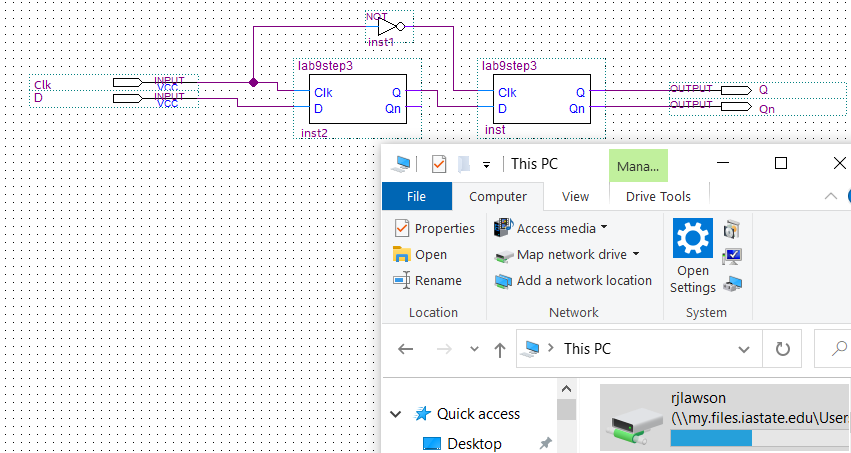
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**4.0** Complete the timing diagram below for your Negative-Edge-Triggered D Flip-Flop.

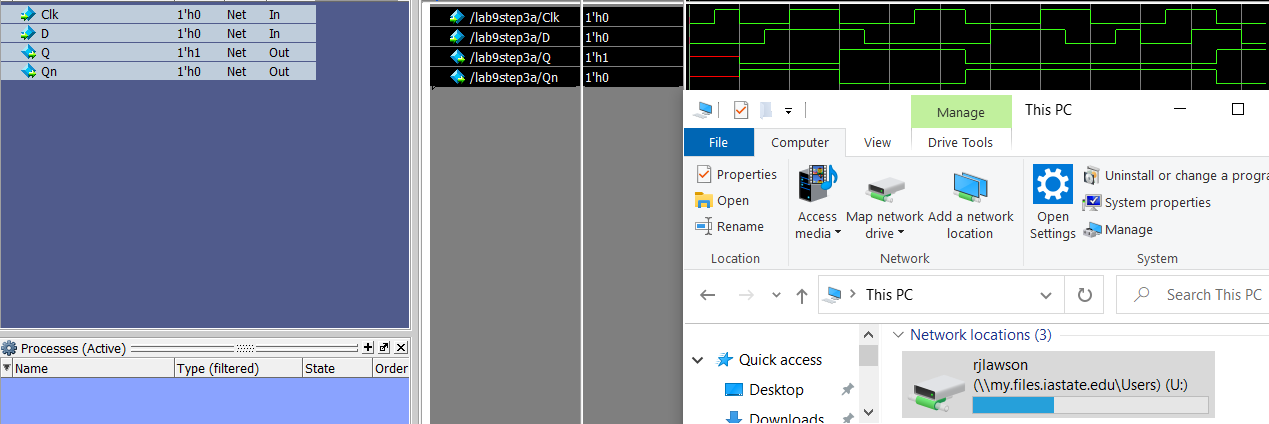
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** | - | \_ | \_ | \_ | - | - | - | - | - | \_ | \_ | \_ | \_ | \_ | \_ | \_ | \_ | \_ | \_ | - | - |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **~Q** | - | - | - | - | \_ | \_ | \_ | \_ | \_ | - | - | - | - | - | - | - | - | - | - | \_ | \_ |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Negative Edge D Flip-Flop Screenshots:**

<<<Insert a screenshot of your Neg. Edge DFF here>>>



<<< Insert a screenshot of your Neg. Edge DFF waveform here>>>

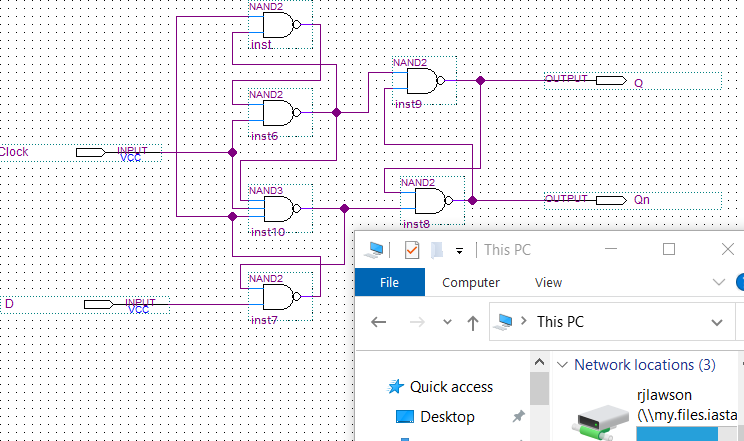


Complete the timing diagram below for your Positive-Edge-Triggered D Flip-Flop.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** | - | \_ | - | - | - | - | - | \_ | \_ | \_ | \_ | \_ | - | - | - | - | - | \_ | \_ | \_ | \_ |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **~Q** | - | - | \_ | \_ | \_ | \_ | \_ | - | - | - | - | - | \_ | \_ | \_ | \_ | \_ | - | - | - | - |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Positive Edge D Flip-Flop Screenshots:**

<<<Insert a screenshot of your Pos. Edge DFF here>>>



<<< Insert a screenshot of your Pos. Edge DFF waveform here>>>

